

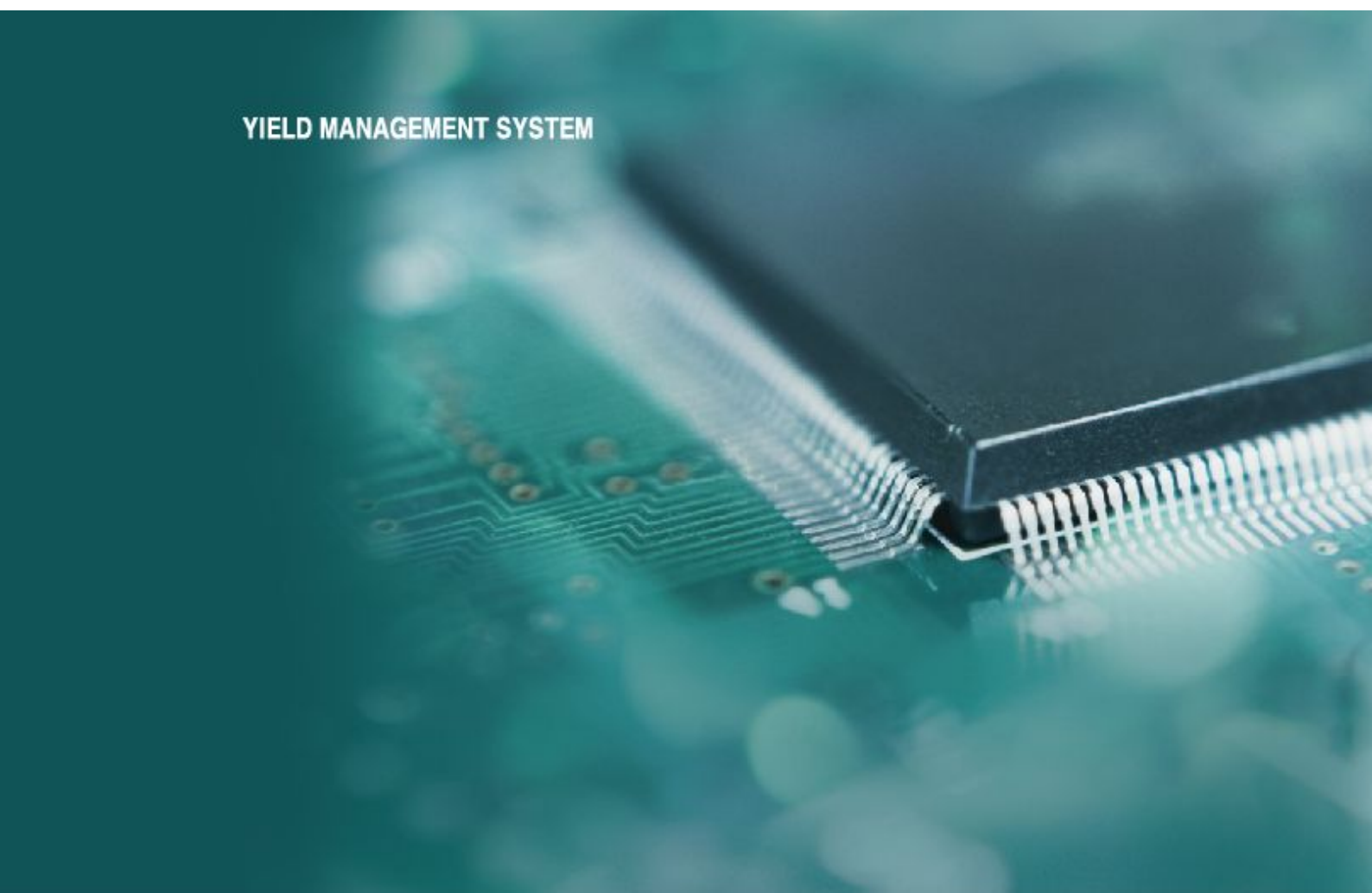


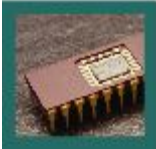
*Optimal YMS (Yield Management System)  
solution for semiconductor yield management!*

*TESTplus provides the total solution  
for semiconductor test floor including automatic data  
collection to the yield analysis applications.*

# TEST Plus

YIELD MANAGEMENT SYSTEM





## Yield Management System

### In order to enhance competitiveness in the semiconductor industry

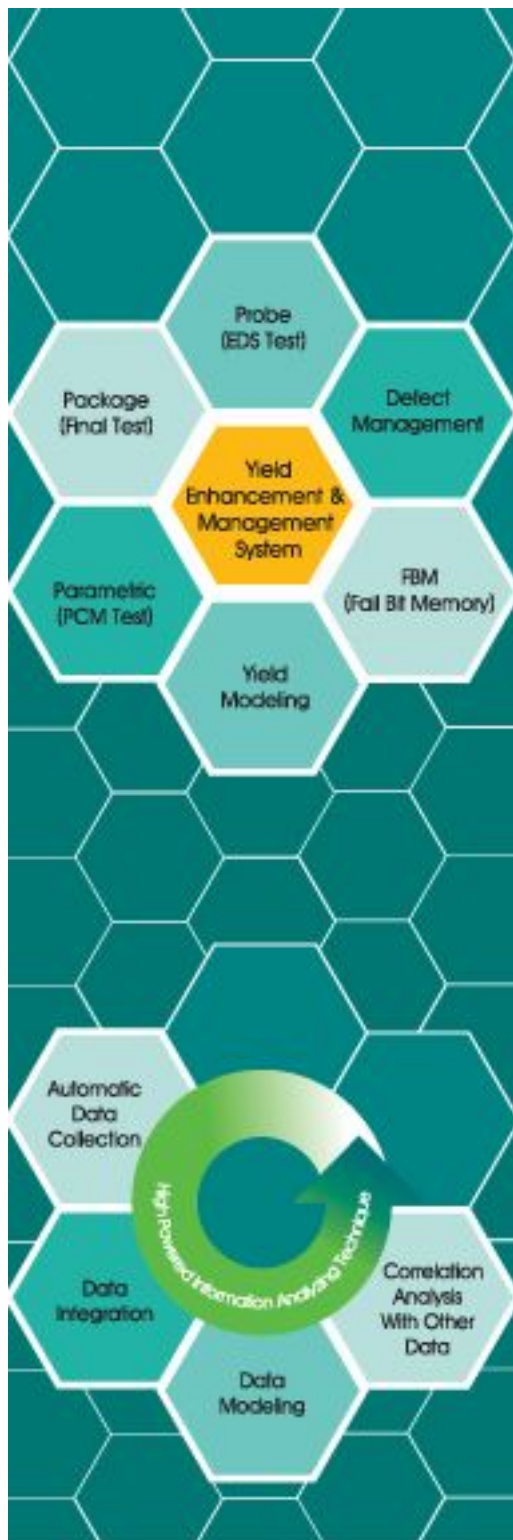
- ▶ Due to complicated manufacturing activities and reduced product lifetime transition in the field of product development to multi-product small/mass Production, the process status should be promptly understood and responded in order to improve the yield quickly.
- ▶ Standardized manufacturing activities and systematic data management are mandatory. Inferiority of quality should be discerned easily and quickly during manufacturing.
- ▶ Improvement criteria for the problems should be presented. Furthermore, similar kind of problems should be reduced in the future through estimation and examination the improvement.
- ▶ The operation ratio which is the most important for productivity and delivery should be exactly understood in order to support to customer's needs.

**TESTplus provides all solutions necessary for the optimum semiconductor test floor.**

# TEST **Plus**

Yield Enhancement &  
Management System

- ▶ Standardizing and managing systematically the data generated from the test floor.
- ▶ Available to take prompt action for abnormal yield by analyzing and reporting test results in real time.
- ▶ Suggesting improvements for productivity improvement and abnormal yields in the test process.
- ▶ Exactly understanding analysis activities and equipment utilization and analysis activities for improving the yield.
- ▶ Simplifying the data analysis procedure; providing high-quality reports; accordingly, stabilizing processes early and predicting the yield.
- ▶ Correlation with other data to analyze data and yield; providing the base for the yield modeling.



TESTplus can provide prompt, efficient and variety Yield Analysis Environment.

Yield Enhancement & Management System is the optimum integrated yield enhancement and management/analysis system which can be applied to various fields of the semiconductor industry including IDM (Integrated Device Manufacture), foundry FAB, assembly/package test (final test) and FABless (Design House).

\* YMS : Yield Enhancement & Management System

## Features & Advantages of TESTplus

### Integration:

- Module Integration: Integration and separation of functions between modules..

- Module Expansion: Customization following the module expansion..
- Additional Function: Addition and Integration of new functions..

Standard Interface : Support of standard development and management method for the test result independently of features of tester, handler or probe..

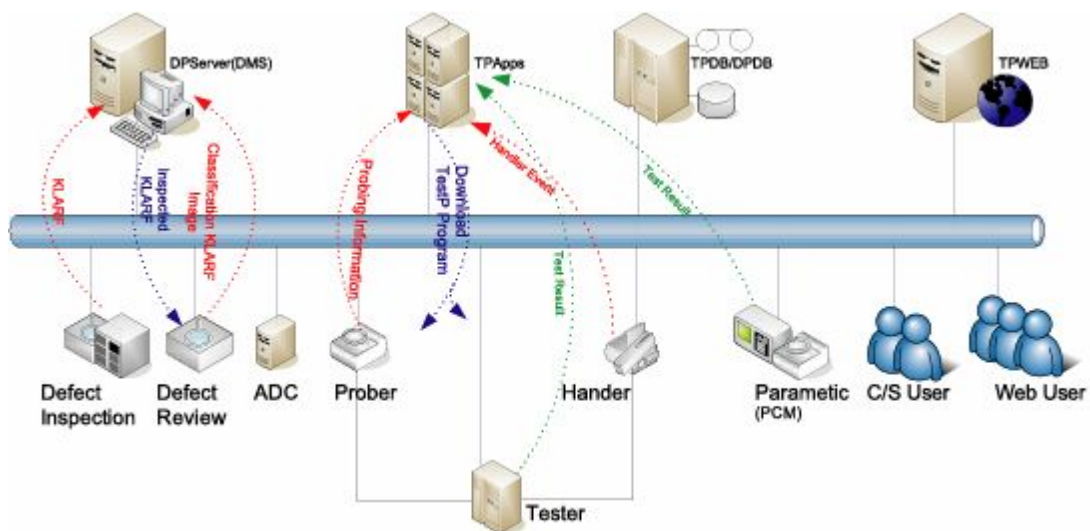
### Flexibility

- Easy Customization : Easy customization of existing functions..
- Easy Upgrade : Easy (cost and time-efficient) upgrade of functions..
- Easy Integration : Correlation analyzing with other systems (MES, DMS, DW)..

### Availability

- Real Size Wafer Map Drawing : Visual analysis and connection with defect and fail bit memory..
- XML Based Data Flow : Extension and diversification of reporting without limitation of platform..
- Fast Activate Function : GPU Acceleration for Wafer Map Drawing & Zoom In/Out..

## TESTplus Architecture

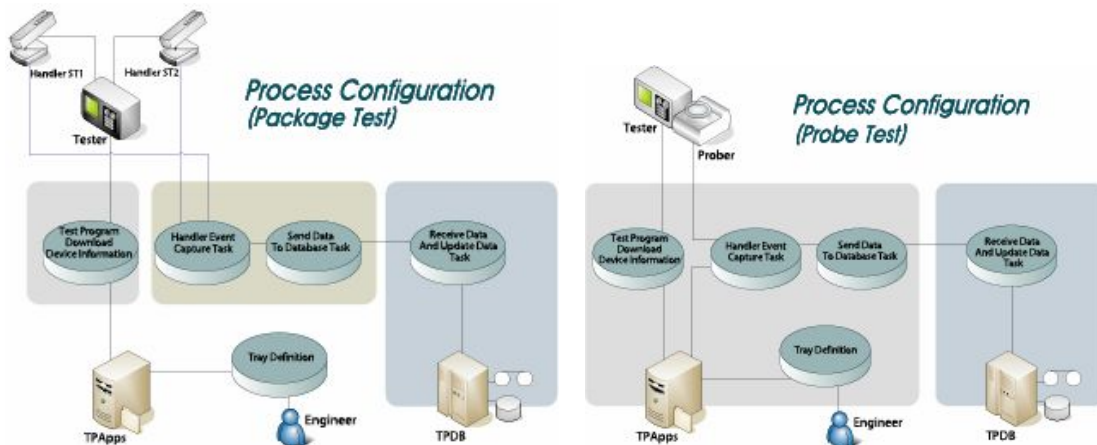


## Features of Technology

- Real Size Wafer Map significantly reduces the gap from the actual wafer size with its high precision design of 1/1000μm. With this, Defect Map, which is the DMS data, can precisely correspond with FBM data.
- DB Server data is serviced to the web and XML, available to providing useful information to the customer.
- Graphic process (Wafer Mapping) uses GPU acceleration to settle bottlenecks for zoom in/out generated during analyzing Wafer Map.
- Human-Less Event Capture binds devices which generate events to RS232 into one IP band, transfers and sends it to TCP.
- Capturing it remotely gives lower investment cost and better service than existing schemes.

## Construction Elements of TESTplus

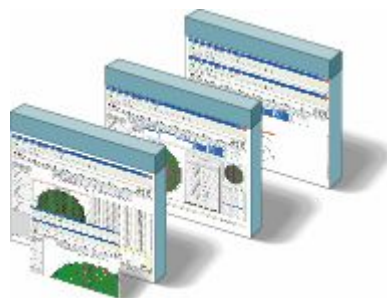
Manager	Data Loader	Probe test Analyzer	Package Test Analyzer	Parametric Analyzer	WEB Reporter
Menu Management	Common File Formatter	Wafer Map Analysis	Bin Data Analysis	Parametric SPC	Summarized Report
Security Management	Human-less Event Capture	Multiple / Cumulated Map	Dut/Tray Data Analysis	Data Analysis	Customer Report
Device Management	XML Generator	Compare Map	Test Efficiency	Chart Analysis	Yield Trend
User Logging	File Transfer	Site Map Analysis	Test Utilization	Outlier Control	Periodic Report
STD Information Definition	DB Loader	Bin Summary	Monitoring (Test OEE)	Short Device Analysis	Statistical Analysis
Test Program Management	Test Driver	Zone Based Analysis	Jam Rate	Correlation Analysis	
	Lot Control	Yield Trend	LIS Data Analysis	Parametric Wafer Map	
		Statistical Yield Analysis	Burn In Data Analysis		
		Probe Card Management	Fail Log Analysis		
		Tester OEE			
		Commonality Study			
		FTA Report			



## Installation Effect

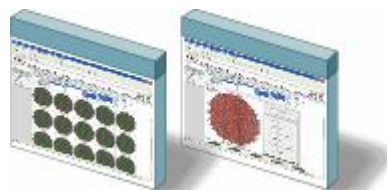
Wafer Map Analysis / FTA(Fail To Attempt Ratio) / Easy Mapping

- High precision when defective data and FBM are overlaid using Real Size Wafer Map; free Zoom In/Out.
- Displaying Repairable Wafer Map in one Wafer Map; Wafer Map Analysis is available in Bin Summary state by simply clicking.



## Multi Wafer Map Drawing

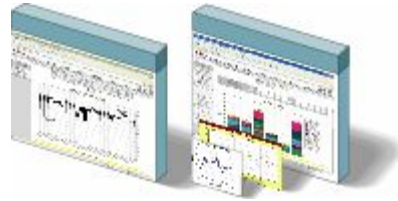
- Understanding/comparing types of defects and patterns in a glance by displaying several wafers multiply or cumulatively.
- Monitoring to find how a certain wafer affect the entire lot or a wafer group via the total cumulated map.



## Various Chart

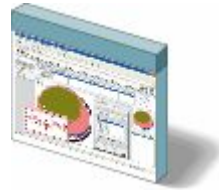
- Providing various types of analysis charts.
- Drilldown in a chart; offering easy

mapping functions such as Bin Summary in Bin Distribution Chart.



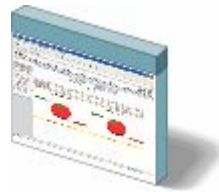
### Parametric Wafer Map

► Illustrating the form of analog results of the probe test or parametric values of the logic device with Wafer Map; accordingly, available to analyze a specific character of defective devices graphically.



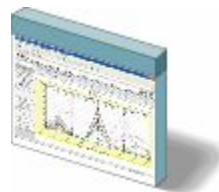
### Tester OEE

► Analyzing the operation rate of test equipment, probe or handler to lead productivity enhancement. Offering reports, charts and more by day, month and equipment.



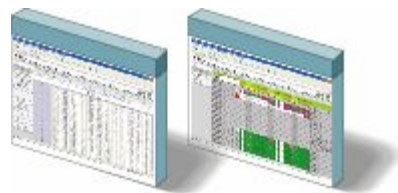
### Package Test

► Analyzing and monitoring the yield trend for the package test result after collecting data directly from the tester or the handler.



### Dut Yield Report Tray Yield Report

► Confirming any differences of dut features in a sheet by monitoring the yield by dut.



## TESTplus Installation Effects

- ▶ Maximizing profits by early yield stabilization of new devices.
- ▶ Reducing the yield loss cost by cutting the yield issue and analysis time.
- ▶ Providing integrated system from data collection to analysis.
- ▶ Reducing fixed and repetitive manual tasks.
- ▶ Sharing information on yield and tester utilization.
- ▶ Analyzing and monitoring operation rate of handler, probe and tester.
- ▶ Preventing quality issues before delivering products to customers.
- ▶ Increasing customer's satisfaction by providing real-time information to customers promptly.
- ▶ Prompt correspondence and flexibility toward changes.
- ▶ Providing accurate and safe information.
- ▶ Increasing ROI due to yield enhancement.
- ▶ Modeling yield.



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